REMARKS

The Office Action dated June 23, 2005 has been received and carefully noted. The above amendments to the claims, and the following remarks, are submitted as a full and complete response thereto.

Claims 1, 11, 12, 13 and 17 have been amended. No new matter has been added, and no new issues are raised which require further consideration and/or search. Claims 18-31 have been allowed. Claims 1 and 3-17 are submitted for consideration.

Applicant wishes to thank the Examiner for indicating the allowance of claims 18-31.

Claims 1, 5-14 and 17 were rejected under 35 U.S.C. 102(e) as being unpatentable over U.S. Patent No. 6,393,548 to Kerstein et al. The rejection is traversed as being based on a reference that neither teaches nor suggests the novel combination of features clearly recited in independent claims 1, 11-13 and 17.

Claim 1, upon which claims 3-10 depend, recites a network switch which includes a data port, a statistics counter, a statistics gathering circuit, and direct memory access circuitry. The data port is used for communicating with a data network. The statistics counter is connected to the data port for monitoring operational parameters associated with the data port. The statistics counter includes statistics registers. The statistics gathering circuit is connected to the statistics counter for reading the statistics registers, and for directly transmitting data from the statistics registers to a remote system memory. The statistics gathering circuit uses the direct memory access circuitry to transmit the

data from the statistics registers to the remote system memory via a Direct Memory Access (DMA) operation. The network switch also includes a configuration register for appropriate port configuration, the configuration register comprising at least one field associated with stacking

Claim 11 recites a network switch including a data port for communicating with a data network and a statistics counter connected to the data port for monitoring operational parameters associated with the data port. The statistics counter includes statistics registers therein. A statistics gathering circuit is connected to the statistics counter for reading the statistics registers, and for directly transmitting data from the statistics registers to a remote system memory. An active counter register is configured to selectively enable statistics gathering from selected ones of the statistics registers.

Claim 12 recites a network switch including a data port for communicating with a data network and a statistics counter connected to the data port for monitoring operational parameters associated with the data port. The statistics counter includes statistics registers therein. A statistics gathering circuit is connected to the statistics counter for reading the statistics registers, and for directly transmitting data from the statistics registers to a remote system memory. The network switch also includes a plurality of data ports and a plurality of statistics counters therein, and wherein each data port of the plurality of data ports has at least one individual statistics counter associated therewith. The network switch further includes an active counter register which is configured to selectively enable statistics gathering by the statistics gathering circuit from selected ones

of the plurality of statistics counters. The network switch also includes a configuration register for appropriate port configuration, the configuration register comprising at least one field associated with stacking

Claim 13, upon which claims 14-16 depend, recites a method of monitoring port activity in a network switch. The method includes the steps of storing port activity data in a statistics register on the network switch and reading the port activity data with a statistics gathering unit. The method also includes the steps of transmitting the port activity data directly to a remote system memory, thereby reconstructing the statistics register in the remote system memory; and accessing the remote system memory with a remote CPU to read the reconstructed statistics register. The method further includes providing appropriate port configuration based on information in a configuration register comprising at least one field associated with stacking.

Claim 17 recites a method of monitoring port activity in a network switch. The method includes the steps of storing port activity data in a plurality of statistics registers on the network switch and reading the port activity data with a statistics gathering unit. The method also includes transmitting the port activity data to a remote system memory to thereby reconstruct the plurality of statistics registers in the remote system memory and accessing the remote system memory with a remote CPU to read the reconstructed statistics registers, wherein the remote CPU accesses the remote system memory to read selected ones of the plurality of statistics registers. The method further includes

providing appropriate port configuration based on information in a configuration register comprising at least one field associated with stacking.

As will be discussed below, the cited prior art reference of Kerstein et al. fails to disclose or suggest the elements of any of the presently pending claims.

Kerstein et al. discloses a network which includes a series of switched transceivers that perform time division multiplexing and time division demultiplexing for data packets transmitted between a multiport switch and 10 Mb/s stations. Col. 4, lines 1-5. The multiple port switch includes a decision making engine, a switching engine, a buffer memory interface, configuration registers, management counters and a MAC protocol interface to support the routing of data packets between the Ethernet ports serving network stations. Col. 4, lines 19-24. The switch includes enhanced functionality to make intelligent switching decisions, to provide statistical network information in the form of management information base objects to an external management entity and interfaces to enable external storage of packet data and switching logic in order to minimize the chip size of the switch. Col. 4, lines 24-32. The switch also includes a management port that enables the external management entity to control overall operations of the switch by a management interface. Col. 4, lines 38-41. The switch further includes a PCI interface connected to a host processor to enable the host process to access the internal IMS registers and the external memory. Col. 4, lines 41-46.

Applicant respectfully submits that the Kerstein et al. fails to disclose all of the elements of independent claims 1, 11-13 and 17. Claims 1 and 11-12, in part, each recites

a configuration register for appropriate port configuration, the configuration register including at least one field associated with stacking. Similarly, each of claims 13 and 17, in part, recites providing appropriate port configuration based on information in a configuration register including at least one field associated with stacking. There is simply no teaching or suggestion in Kerstein et al. of a network switch which includes a configuration register for appropriate port configuration, the configuration register including at least one field associated with stacking as recited in claims 1 and 11-12. Similarly, there is simply no teaching or suggestion in Kerstein et al. of providing appropriate port configuration based on information in a configuration register including at least one field associated with stacking as recited in claims 13 and 17.

Claims 1 and 11-12, in part, each recites that a statistics counter is **connected to** the data port for monitoring operational parameters associated with the data port, the statistics counter includes statistics registers and a statistics gathering circuit is **connected to** the statistics counter for reading the statistics registers and for directly transmitting data from the statistics registers to a remote system memory. There simply is no teaching of suggestion in Kerstein et al. of a statistics counter that is **connected to** a data port. Col. 4, lines 6-10 of Kerstein et al. merely teaches a transceiver interface that transmits and receives data packets to and from each switch transceiver across a single serial non-return to zero interface. Figure 1 of Kerstein et al, further shows media independent interfaces 28 that provide a connection to physical devices. See. Col. 3, lines 49-67. As such, Applicant submits that the transceiver interface and the media independent interface

of Kerstein are simply not the same is the statistic counter that is **connected to** the data port, that is used for monitoring operational parameters associated with the data port and that includes statistics registers as recited in claims 1 and 11-12.

Furthermore, claims 1 and 11-12, recite in part that a statistics gathering circuit is **connected to** the statistics counter for reading the statistics registers and for directly transmitting data from the statistics registers to a remote system memory. Although Kerstein et al. teaches a RAM/SDRAM interface that provides access to an external memory, there is no teaching or suggestion in Kerstein et al. that the RAM/SDRAM interface is **connected to** a statistic counter in order for the RAM/SDRAM interface to read associated statistic registers and directly transmit data from the registers to a remote memory as recited in claims 1, 11 and 12. Kerstein et al. also discloses in Col. 10, lines 1-6, that the external memory includes a MIB counter region that contains all per port statistic which are updated periodically by the switch. However, Kerstein et al. does not disclose how the MIB counter region is updated. There is no teaching or suggestion in Kerstein et al. that the MIB counter region is updated by a statistics gathering circuit that is connected to the statistics counter, that reads the statistics registers and that directly transmits data from the statistics registers to the a remote system memory as recited in claims 1, 11 and 12. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. §102(e) should be withdrawn because Kerstein et al. simply fails to teach or suggest each of the elements of claims 1, 11-13 and 17 and hence, dependent claim 5-10 and 14 thereon.

Claims 3-4 and 15-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over Kerstein et al. in view of U.S. Patent No. 5,909,564 to Alexander et al. The rejection is traversed as being based on references that neither teach nor suggest the novel combination of features clearly recited in independent claims 1 and 13 upon which claims 3-4 and 15-16 are dependent.

Alexander et al. discloses an Ethernet frame switch which has an Ethernet switch processor coupled to a multi-channel direct memory access (DMA) controller, medium access control (MAC) interface logic blocks, an external memory controller and an expansion bus interface logic block. Col. 2, line 64-Col 3, line 2. Ethernet frame data is accepted from terminals by the MAC interface logic blocks and buffered in the associated FIFO. The DMA controller transfers the data to external memory and notifies the Ethernet switch processor of the presence of a received frame. Col. 3, lines 9-13. After the processor inspects the frame, if the target of the frame is determined to be an end-system associated with some other MAC interface port, the Ethernet switch processor causes the DMA controller to transfer the frame data out of the external memory to the MAC interface port. Col. 3, lines 14-23.

Applicant respectfully submits that Alexander et al. fails to cure the deficiencies of Kerstein et al. Applicant submits that Alexander et al. in no way discusses or even suggests a configuration register for appropriate port configuration, the configuration register including at least one field associated with stacking. Furthermore, Alexander et al. does not teach or suggest statistic counters that are connected to data ports and a

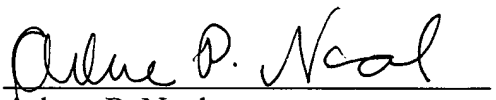
statistic gathering circuit that directly transmits information from associated statistics registers to a remote system memory where the statistics registers are reconstructed and accessed by a remote CPU that reads the reconstructed statistics register, wherein the remote CPU accesses a selected portion of the statistic register in the remote system memory as recited in claims 1 and 13. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. §103(a) should be withdrawn because neither Kerstein et al. nor Alexander et al., whether taken singly or combined, teaches or suggests each feature of claims 1 and 13 and hence, dependent claim 3-4 and 15-16 thereon.

As previously noted, each of claims 1 and 3-17 recited subject which is neither disclosed nor suggested in the cited prior art reference. It is therefore respectfully requested that all of claims 1 and 3-17 be allowed, in addition to allowed claims 18-31, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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